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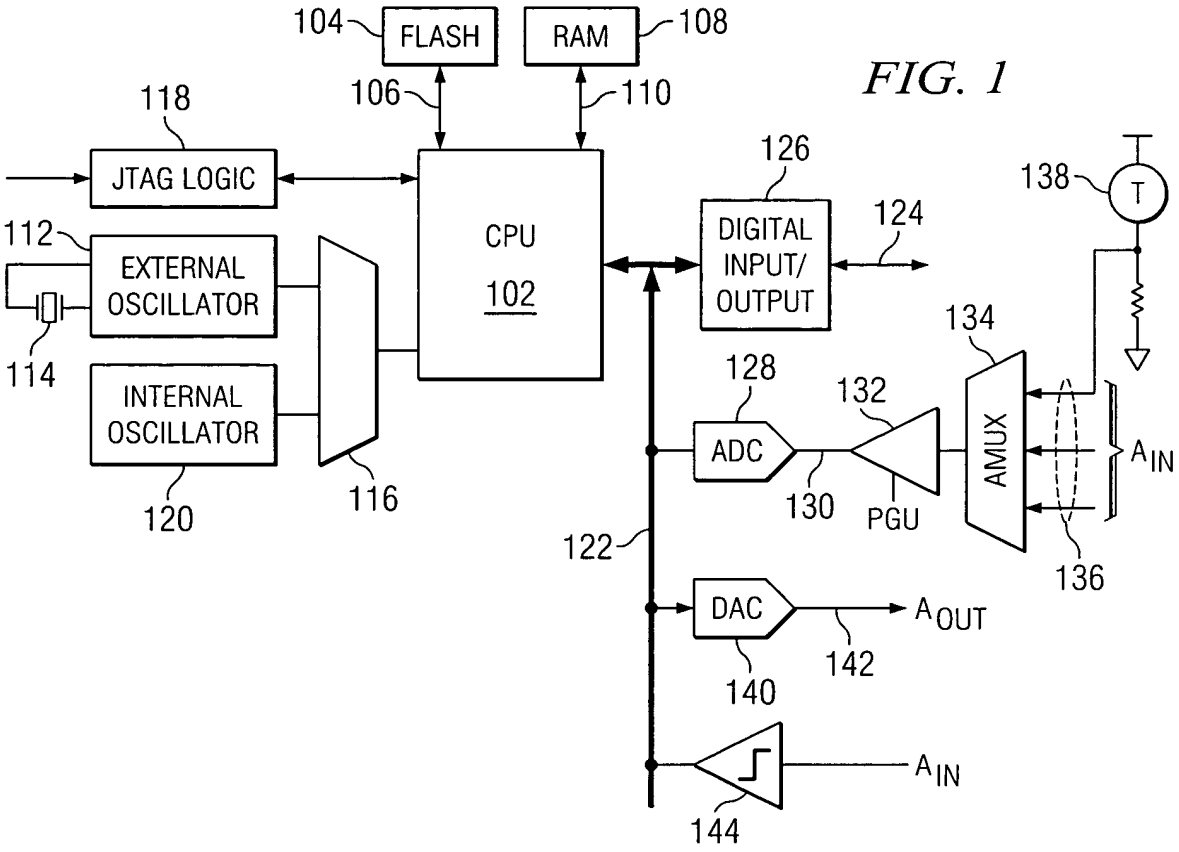


FIG. 1

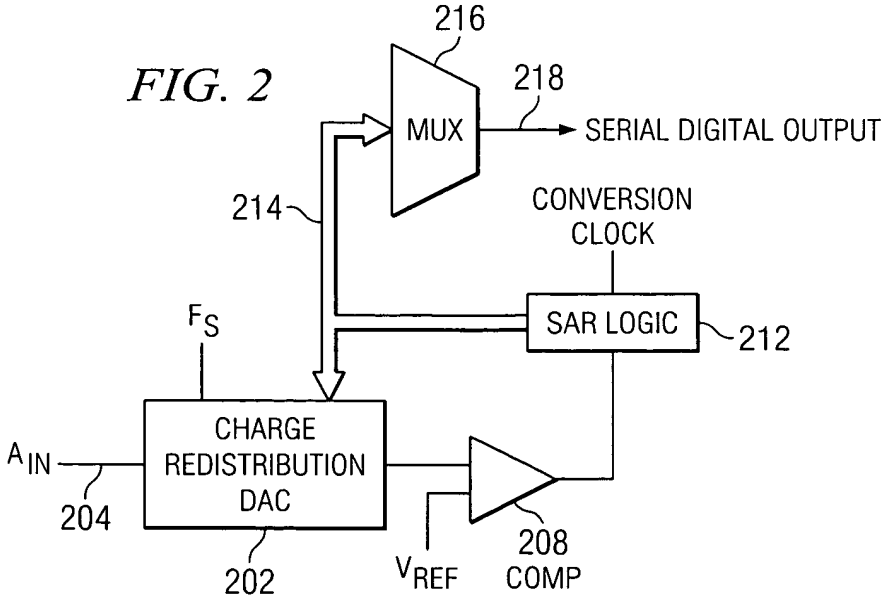


FIG. 2

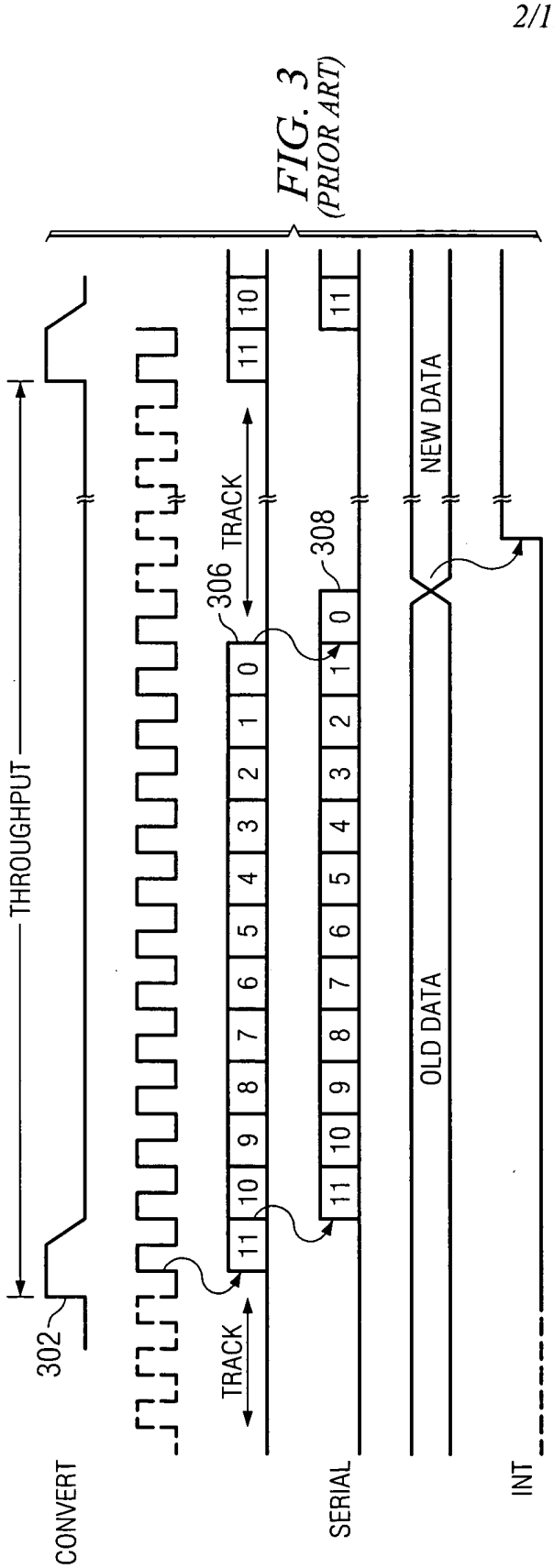


FIG. 3
(PRIOR ART)

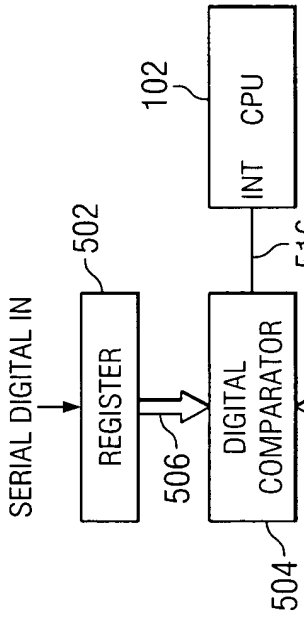


FIG. 5

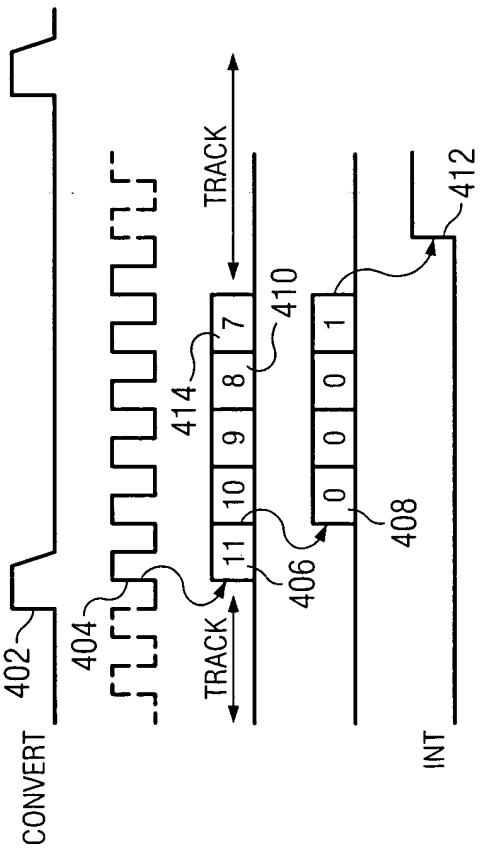


FIG. 4

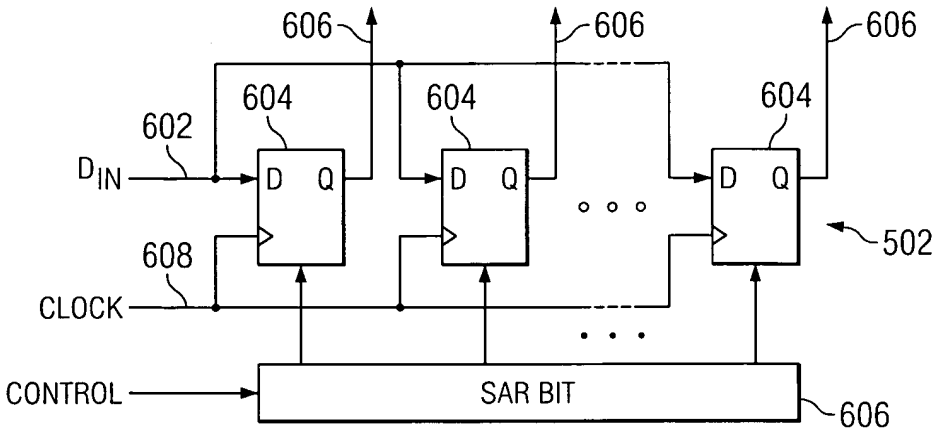


FIG. 6

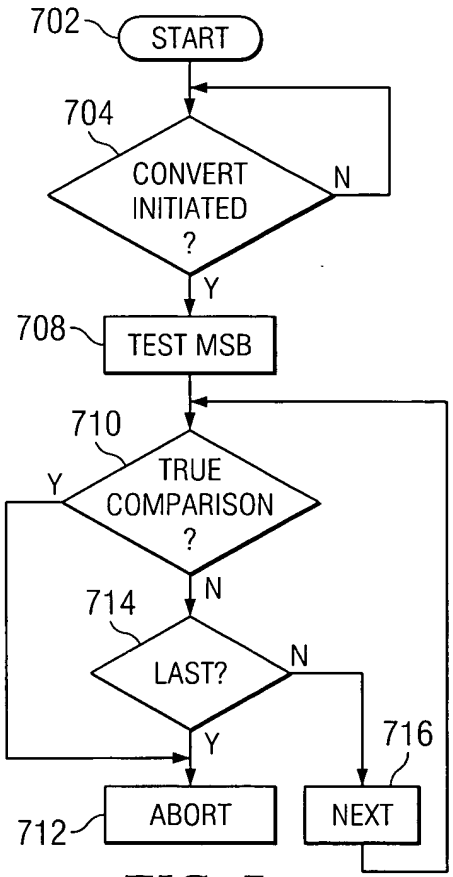


FIG. 7

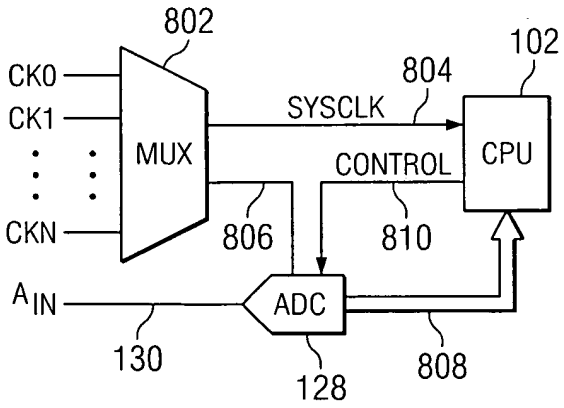


FIG. 8

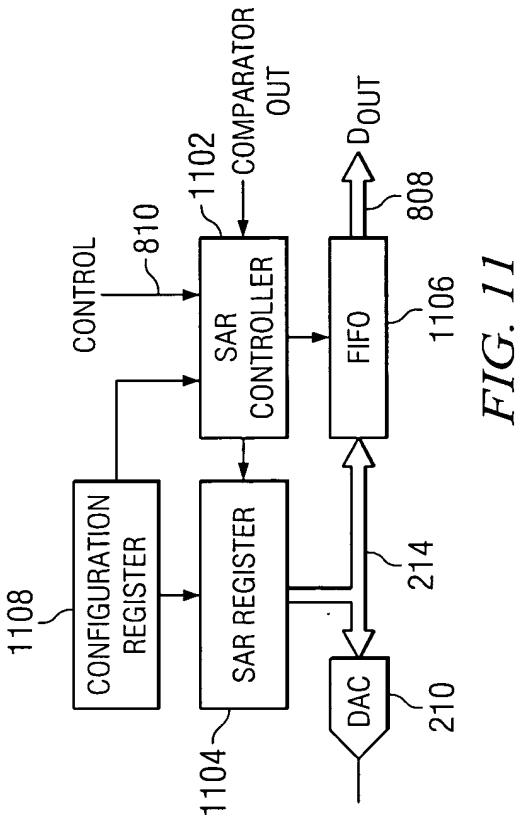


FIG. 11

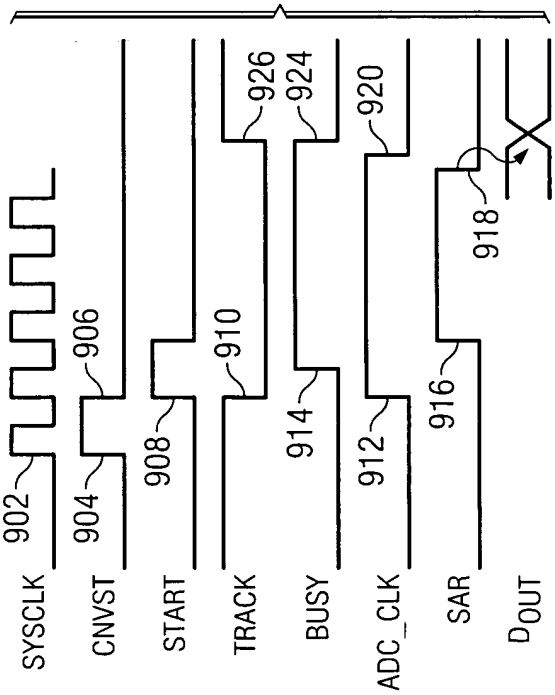


FIG. 9

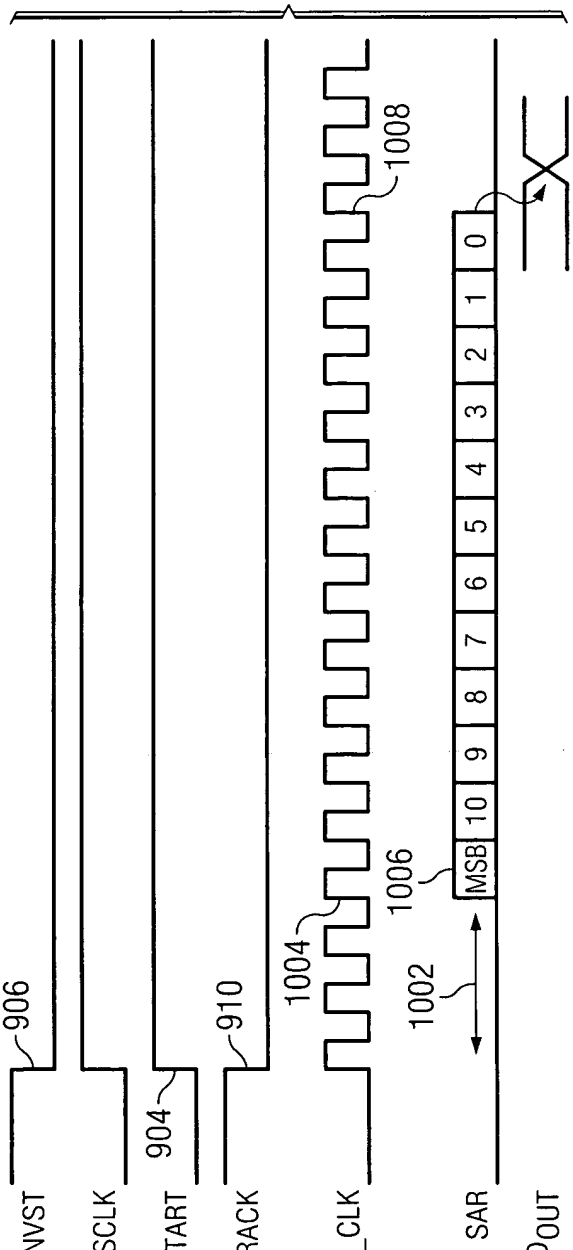


FIG. 10

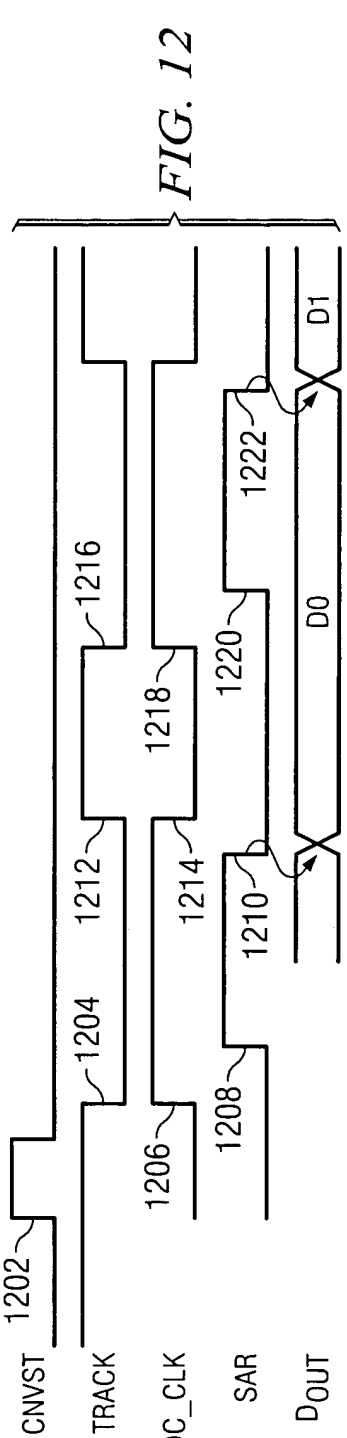

CNVST
TRACK
ADC_CLK
SAR
DOUT
1202
1204
1206
1208
1210
1212
1214
1216
1218
1220
1222
D0
D1

FIG. 12

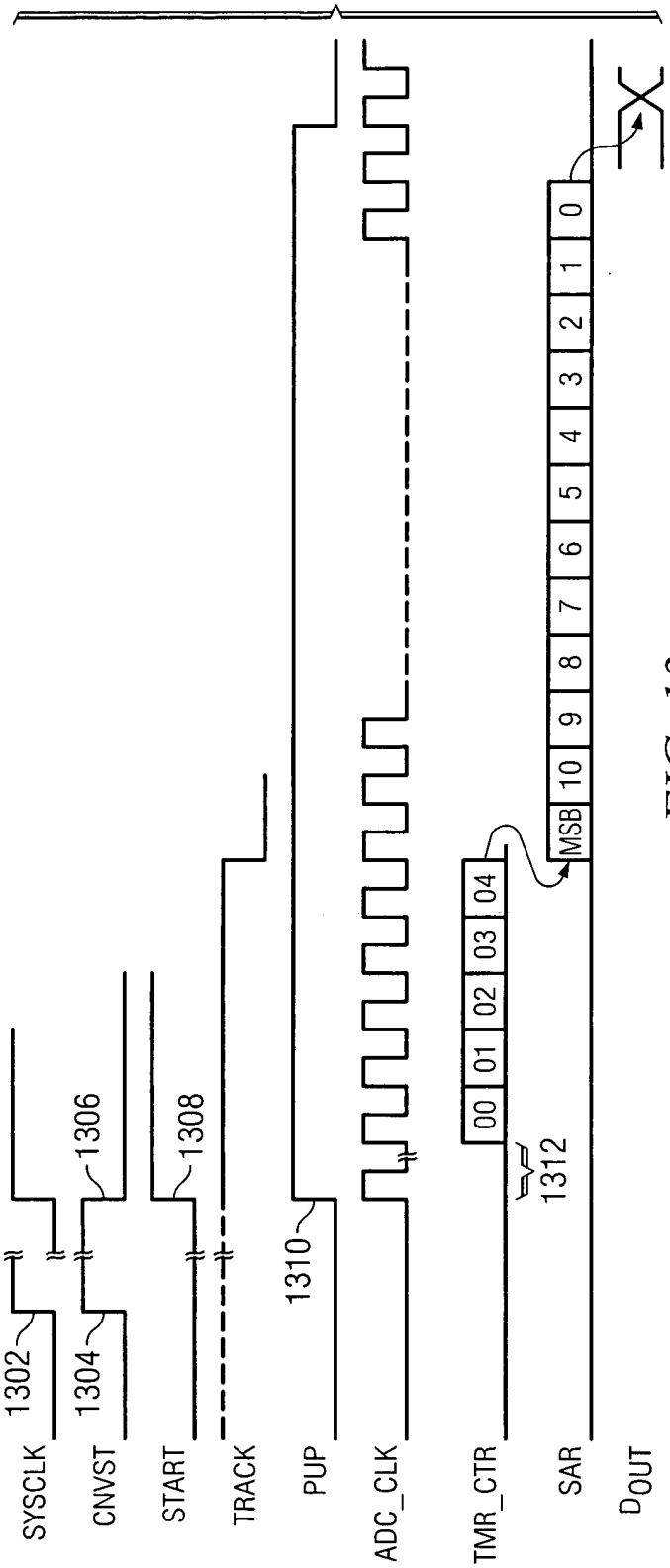

SYSCLK
CNVST
START
TRACK
PUP
ADC_CLK
TMR_CTR
SAR
DOUT
1302
1304
1306
1308
1310
1312
00
01
02
03
04
MSB
10
9
8
7
6
5
4
3
2
1
0

FIG. 13

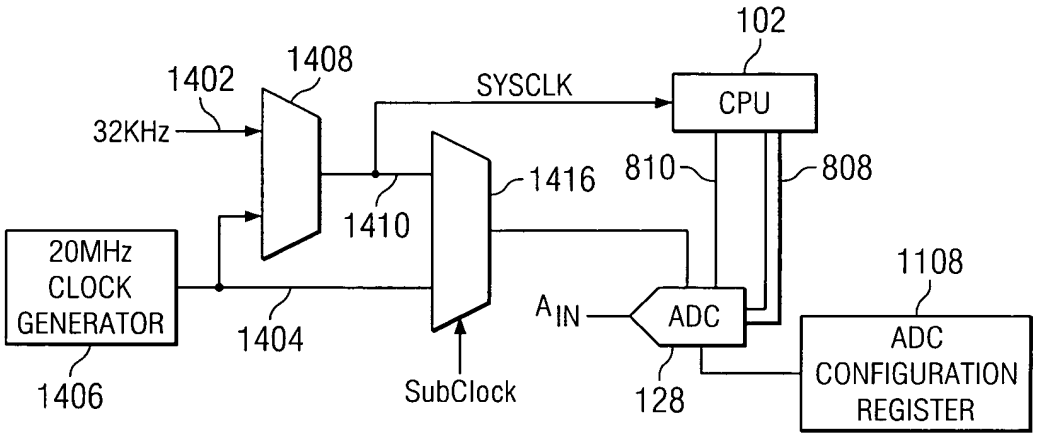


FIG. 14

ADC0TK

ADCTM0 ADCTM1
POSTTK
PRETK
ADCPWR0 ADCPWR1 ADCPWR2 ADCPWR3

FIG. 15a

ADC0CF

CALEN
ADCRPT0 ADCRPT1
ADCSC0 ADCSC1 ADCSC2 ADCSC3 ADCSC4

FIG. 15b

ADC0CN

ADCCM0 ADCCM1
ADCJST
ADCWINT
ADBUSY
ADCINT
BURSTEN
ADCEN

FIG. 15c

FIG. 16

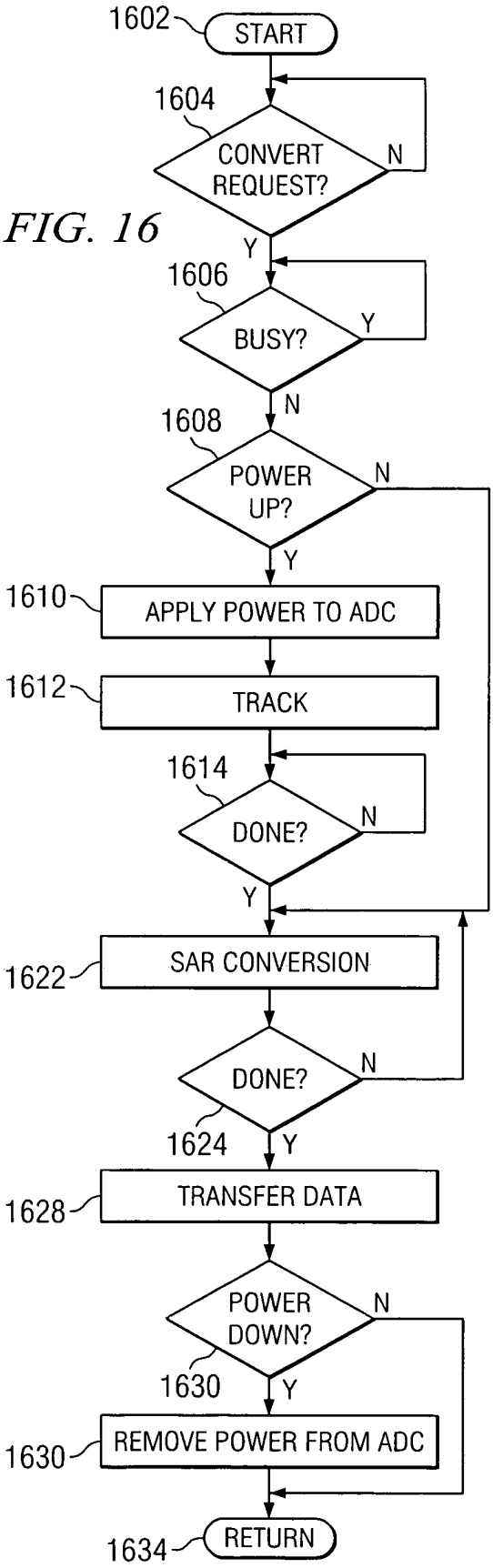
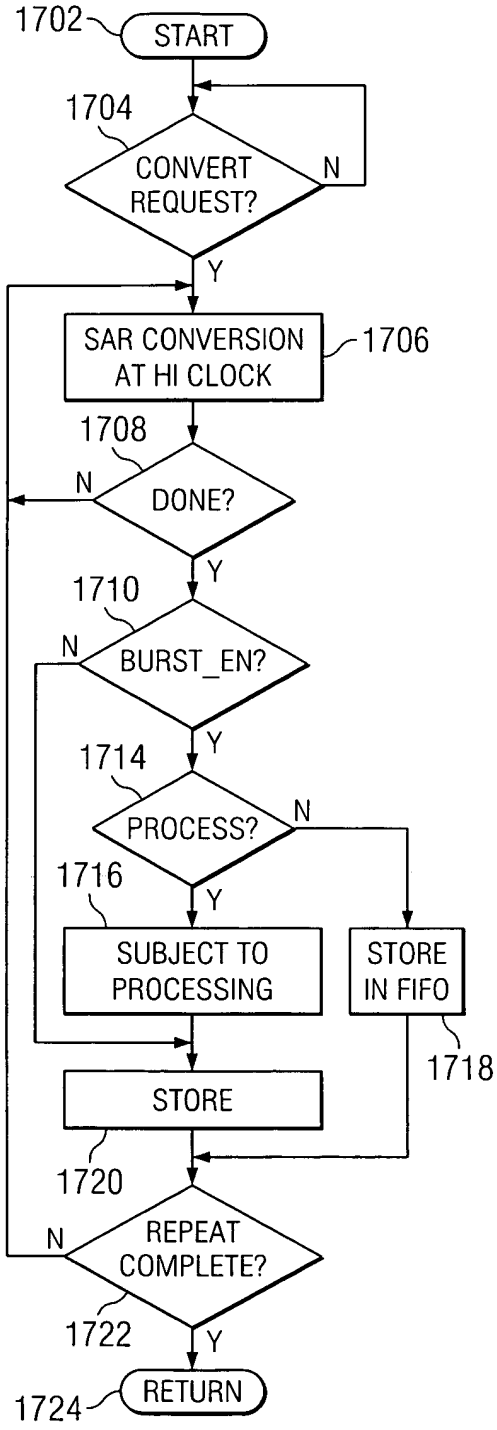

1602
START
1604
CONVERT REQUEST?
N
Y
1606
BUSY?
Y
N
1608
POWER UP?
N
Y
1610
APPLY POWER TO ADC
1612
TRACK
1614
DONE?
N
Y
1622
SAR CONVERSION
DONE?
N
1624
Y
1628
TRANSFER DATA
POWER DOWN?
N
1630
Y
1630
REMOVE POWER FROM ADC
1634
RETURN

FIG. 17


1702
START
1704
CONVERT REQUEST?
N
Y
SAR CONVERSION AT HI CLOCK
1706
1708
DONE?
N
Y
1710
BURST_EN?
N
Y
1714
PROCESS?
N
Y
1716
SUBJECT TO PROCESSING
STORE IN FIFO
1718
STORE
1720
REPEAT COMPLETE?
N
1722
Y
1724
RETURN

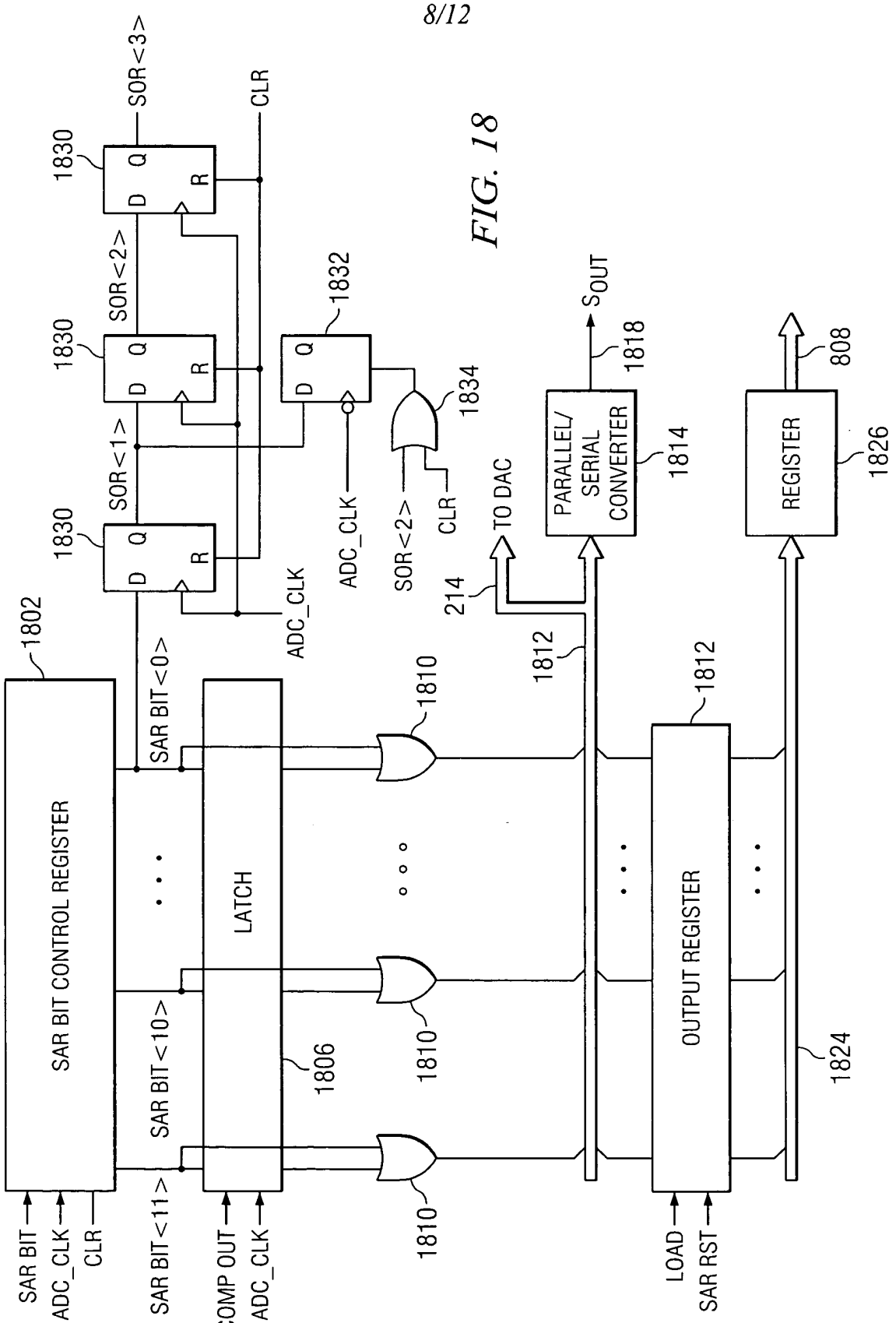

SAR BIT
ADC_CLK
CLR
SAR BIT<11>
COMP OUT
ADC_CLK
LOAD
SAR RST
SAR BIT CONTROL REGISTER
1802
SAR BIT<0>
SAR BIT<10>
LATCH
1806
1810
1812
1824
OUTPUT REGISTER
PARALLEL/ SERIAL CONVERTER
1814
SOUT
1818
REGISTER
1826
808
TO DAC
214
SOR<2>
CLR
ADC_CLK
1834
1832
1830
SOR<1>
SOR<2>
SOR<3>
D
Q
R

FIG. 18

FIG. 19

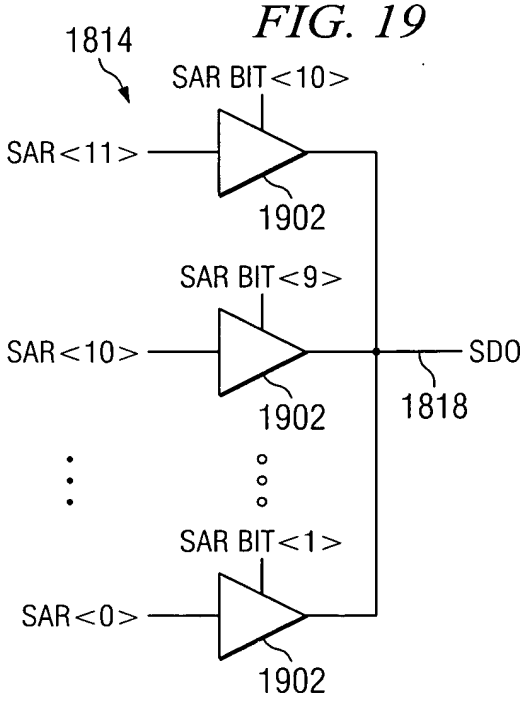


FIG. 20

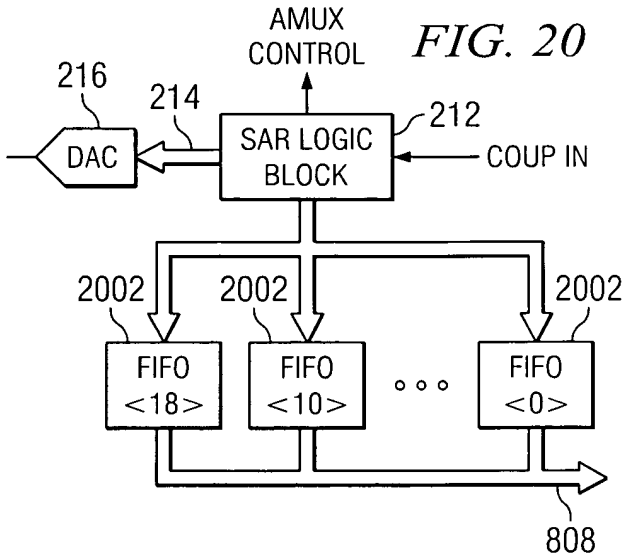
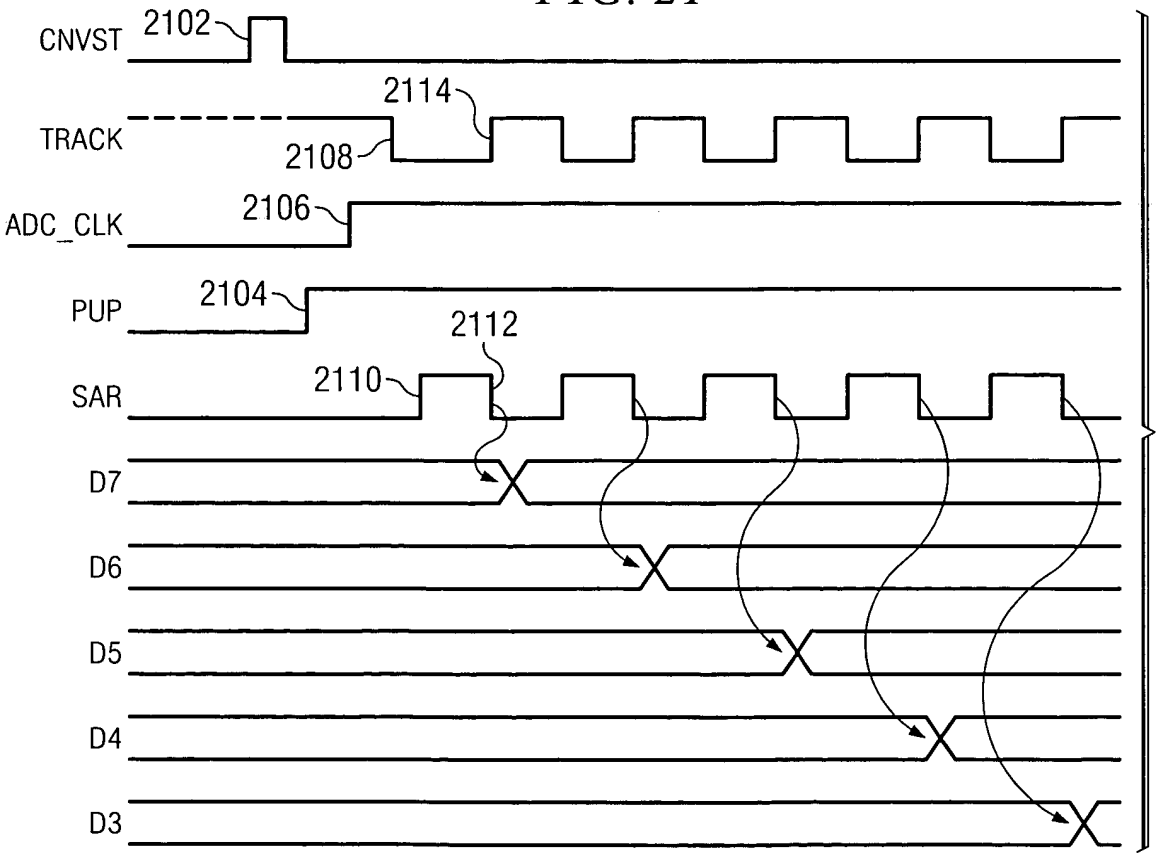


FIG. 21



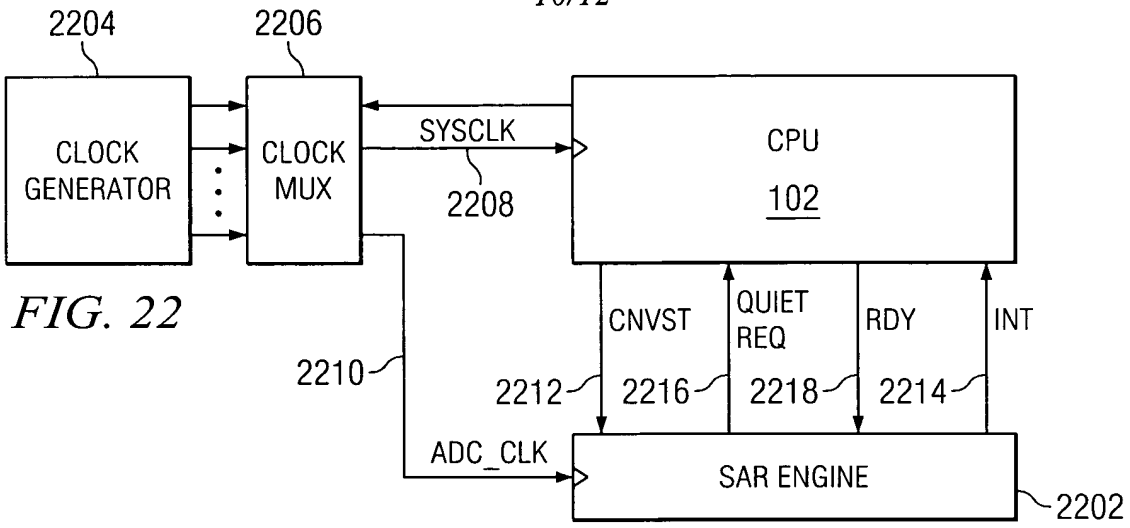


FIG. 22

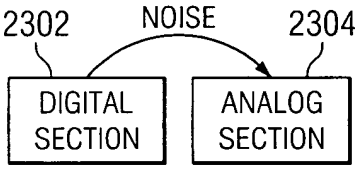


FIG. 23

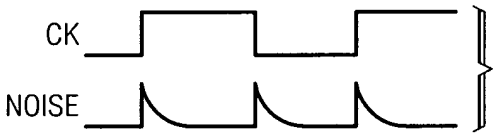


FIG. 24

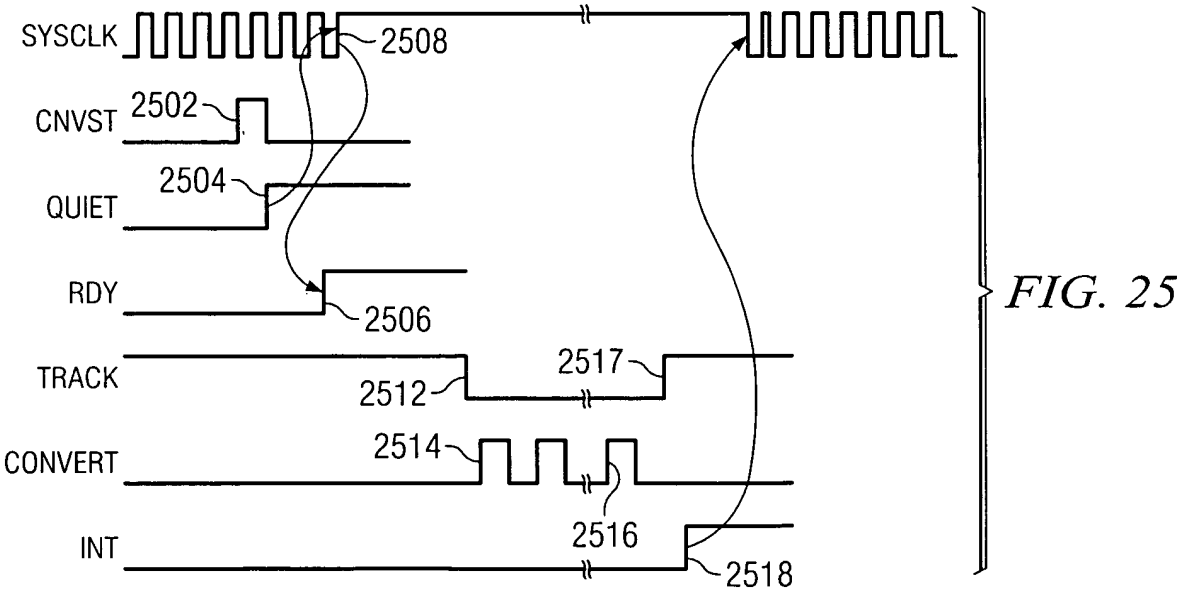


FIG. 25

FIG. 26

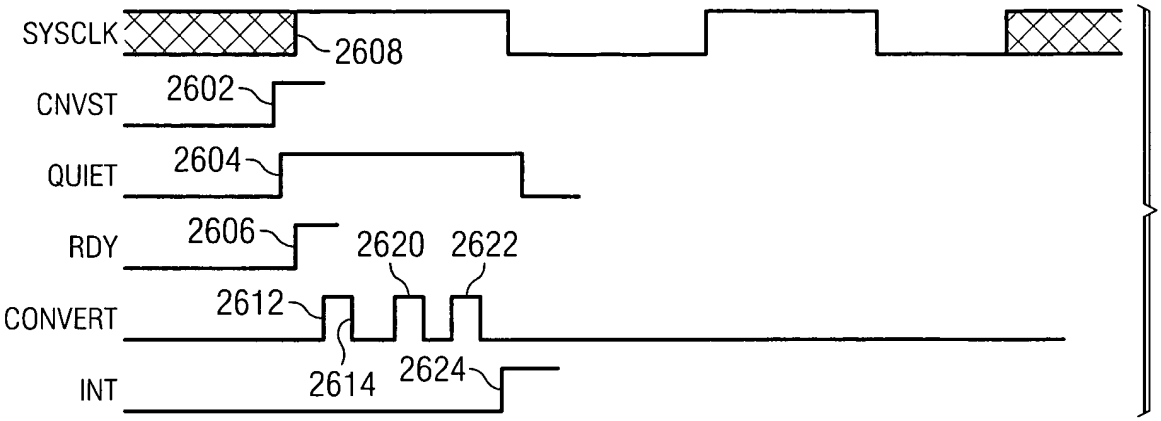
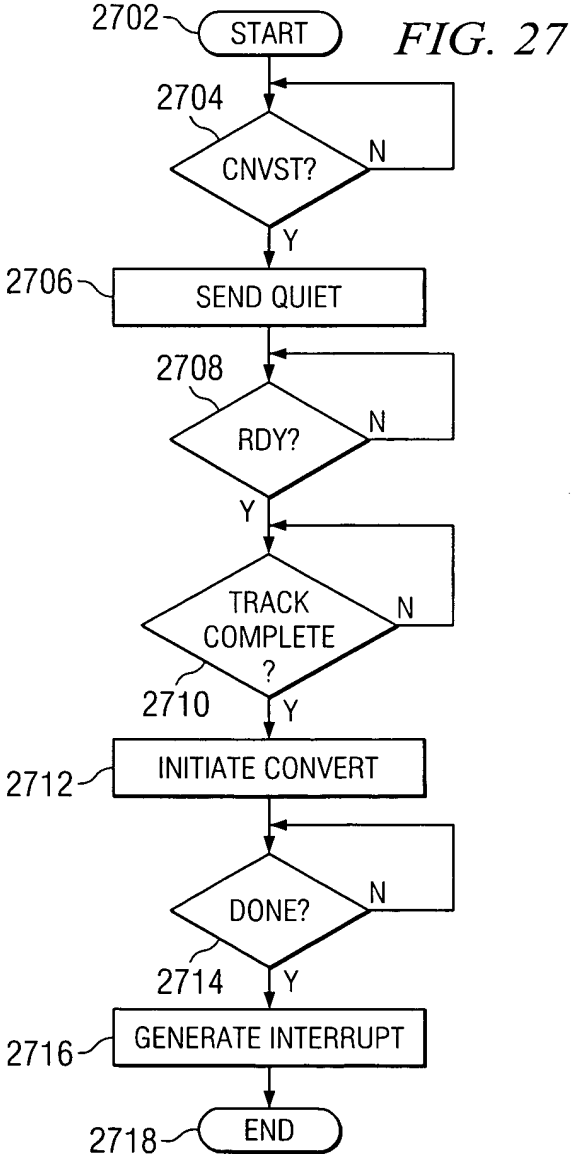

SYSCLK
2608
CNVST
2602
QUIET
2604
RDY
2606
2620
2622
CONVERT
2612
2614
2624
INT

FIG. 27


2702
START
2704
CNVST?
N
Y
2706
SEND QUIET
2708
RDY?
N
Y
TRACK COMPLETE ?
N
2710
Y
2712
INITIATE CONVERT
DONE?
N
2714
Y
2716
GENERATE INTERRUPT
2718
END

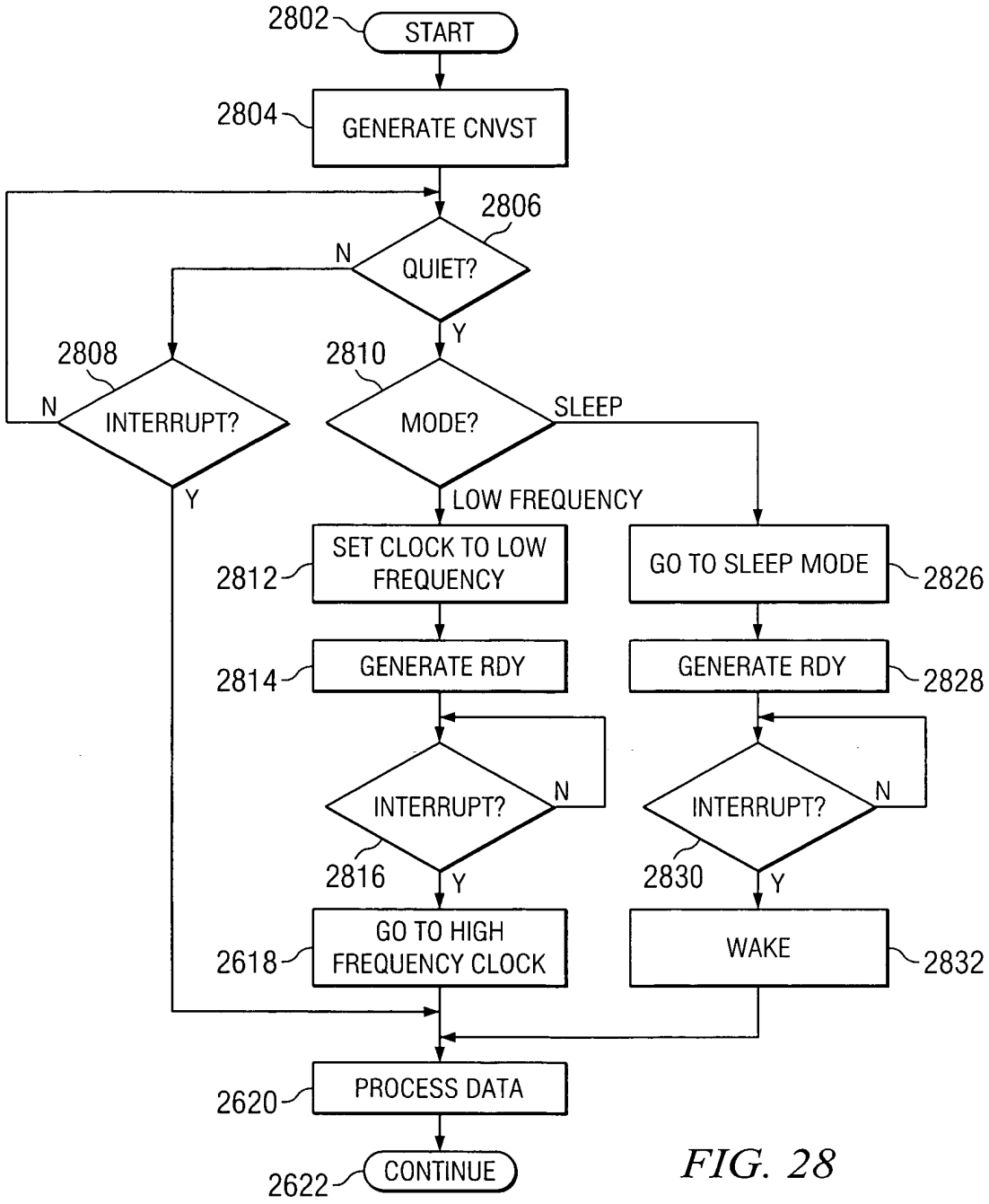

2802
START
2804
GENERATE CNVST
2806
QUIET?
N
Y
2808
INTERRUPT?
N
Y
2810
MODE?
SLEEP
LOW FREQUENCY
2812
SET CLOCK TO LOW FREQUENCY
2814
GENERATE RDY
INTERRUPT?
N
2816
Y
2618
GO TO HIGH FREQUENCY CLOCK
2826
GO TO SLEEP MODE
2828
GENERATE RDY
INTERRUPT?
N
2830
Y
2832
WAKE
2620
PROCESS DATA
2622
CONTINUE

FIG. 28